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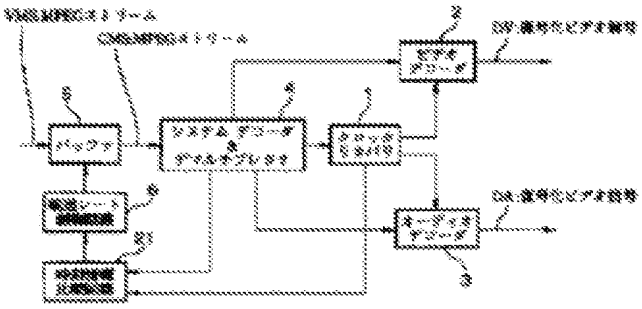
Abstract:
PROBLEM TO BE SOLVED: To receive a stable moving picture experts group(MPEG) stream by synchronizing the reference clock of a decoder system on the side of reception with a clock on the side of transmission without considerably deviating it even on the condition that the jitter of the MPEG stream to be received suddenly gets large. SOLUTION: MPEG data to be received are stored in a buffer 5. A transfer rate control circuit 6 transfers the MPEG data stored in the buffer 5 to a system decoder and demultiplexer 4 at a fixed transfer rate. A time information comparator circuit 21 compares time information contained in the MPEG data read out of the buffer 5 with time shown by a reference clock to be used for the timing control of a decoder in the system decoder and demultiplexer 4 and based on the compared result, a command to change the transfer rate is supplied to the transfer rate control circuit 6.



JPO Machine translation abstract:
(57) **Abstract**
SUBJECT The jitter of the MPEG stream received does not make the reference clock of the decoder system of a receiver produce a big gap also under the situation of becoming large suddenly, but makes it synchronize with the clock of the transmitting side, and receives the stable MPEG stream.
Means for SolutionMPEG data received is stored in the buffer 5. The transfer rate control circuit 6 transmits MPEG data stored in the buffer 5 to the system decoder & demultiplexer 4 with a fixed transfer rate. Time information included in MPEG data in which the time information comparison circuit 21 is read from the buffer 5, Time which a reference clock used for timing control of a decoder in the system decoder & demultiplexer 4 shows is compared, and instructions of a purport that a transfer rate should be changed based on a comparison result are supplied to the transfer rate control circuit 6.

Claim(s)
Claim 1 An MPEG data transfer control circuit comprising:
A buffer which stores MPEG data received one by one.
A transfer rate control circuit which transmits MPEG data stored in said buffer to a decoder with a fixed transfer rate.
A time information comparison circuit which supplies instructions of a purport that time which time information included in MPEG data read from said buffer and a reference clock used for timing control of said decoder show is compared, and said transfer rate should be changed based on a comparison result to said transfer rate control circuit.

Claim 2 Said time information comparison circuit, Supplying instructions which raise said transfer rate when time which time information included in a packet read from said buffer and a reference clock used for timing control of said decoder show is **beyond specified value** far apart and which are ordered or dropped to said transfer rate control circuit. The MPEG data transfer control circuit according to claim 1 by which it is characterized.
Claim 3 Said time information comparison circuit writes periodically difference with time which time information included in a packet read from said buffer and a reference clock used for timing control of said decoder show in a time information store circuit, According to a temporal response of each difference memorized in said time information store circuit, an increasing rate or a downward rate of said transfer rate is determined, The MPEG data transfer control circuit according to claim 1 supplying instructions which raise said transfer rate according to the determination concerned, and which are ordered or dropped to said transfer rate control circuit.

Detailed Description of the Invention
0001

Field of the Invention This invention relates to the MPEG data transfer control circuit for performing control for supplying to a decoder the MPEG data which is applied to an MPEG decoder, especially is received via a transmission line at a fixed rate.

0002

Description of the Prior Art As the International Standard about digital video (video) coding (compression), voice (audio) coding, and its multiplex and separation system, There is an MPEG (Moving PictureExperts Group) standard (ISO/IEC DIS 11172/13818) used in common in fields, such as a storage medium, communication, and broadcast. MPEG1 used for this MPEG standard by storage media, such as CD-ROM (CompactDisk Read Only Memory), There is MPEG 2 which broadcast and the use in a telecommunications sector besides the application of this MPEG1 are considered, and is used with broad application. The MPEG 2 program stream (PS:ProgramStream) which can constitute one program in a stream like **this MPEG 2** MPEG1, There are two kinds of systems called the MPEG2 transport stream (TS:Transport Stream) which can constitute two or more programs in a stream. Since especially MPEG 2-TS can summarize two or more programs to one stream, it can respond to television broadcasting etc. MPEG 2-TS is provided with flexibility, a scramble function, etc. of program organization so that it may harness this advantage.

0003 Next, the MPEG system which performs the data communications corresponding to MPEG explained above is explained. In this MPEG system, the video signal and audio signal which digitized at the transmitting side are compressed once, and it transmits to a receiver through media, such as a network and a hard disk. And in a receiver, the original video signal and audio signal are restored from the compressed data. Here, irreversible encoding is used for the coding mode of MPEG in order to drop the amount of information as much as possible. For this reason, in a receiver, the original video signal and audio signal cannot be restored thoroughly. However, using well the weak point of human being's vision and an acoustic sense, the amount of information is dropped on the coding mode of MPEG to such an extent that he hardly notices human being. However, if the transfer rate of the MPEG day evening becomes low (it is got blocked and the amount of information becomes small), the difference with the original image and fundamental tone voice which can be checked to human being will become large. The above is an outline of an MPEG system.

0004 Drawing 4 is a block diagram showing the basic constitution of the MPEG system explained above. Drawing 5 is a block diagram showing the example of composition of the decoder system 9 in an MPEG system. Drawing 6 is a block diagram showing the composition of the clock recovery 1 in the decoder system 9.

0005 In drawing 4, the MPEG encoder system 7 includes an encoder, a buffer, a clock control circuit, etc. Audio input A.I. Artificial Intelligence which is input video VI and the audio signal which are picture signals is inputted into this encoder system 7. And the MPEG encoder system 7 compresses these input, and outputs the compressed MPEG stream (MPEG coding was carried out). This MPEG stream is inputted into the MPEG decoder system 9 through a network or the video server 8. The MPEG decoder system 9 decodes these compression streams, and outputs the video output VO and the audio output AO.

0006 By the way, in an MPEG system, signal transmission between the input edge of the MPEG encoder system 7 and the outgoing end of the MPEG decoder system 9 must always be performed by fixed delay. Because, it is necessary to transmit a video signal and an audio signal to real time by a waveform as it is in an MPEG system. For example, when its attention is paid to the video or the audio signal inputted into the encoder system 7, Each signal exactly inputted into ... in 1 second, 2 seconds, and 3 seconds from the input start point in time of a top signal must be exactly outputted to ... in 1 second, 2 seconds, and 3 seconds from the output start point in time of a top signal, also when outputted from the decoder system 9.

0007 In an MPEG system, signal transmission between the outgoing end of the encoder system 7 and the input edge of the decoder system 9 must also always be performed by fixed delay. Because, include the time information (time information intended with the encoder) as which the encoder system 7 expresses the timing of the clock by the side of an encoder in an MPEG system into an MPEG stream, and it transmits, In the decoder system 9, the reference clock used for control of the reproducing output timing of video or an audio is synchronized with the clock by the side of an encoder by receiving this time information (in addition, this synchronization control is mentioned later). Therefore, if the delay of the signal transmission between the outgoing end of the encoder system 7 and the input edge of the decoder system 9 is not fixed, the receiving timing of the hour entry in the decoder system 9 will come apart, and the reference clock by the side of a decoder will shift from the clock by the side of an encoder. Unless signal transmission between the outgoing end of the encoder system 7 and the input edge of the decoder system 9 is performed for fixed delay, signal transmission between the input edge of the MPEG encoder system 7 and the outgoing end of the MPEG decoder system 9 cannot be performed for fixed delay, either. Therefore, signal transmission between the outgoing end of the encoder system 7 and the input edge of the decoder system 9 must always be performed for fixed delay as above-mentioned.

0008 However, transmission of an MPEG stream is actually performed through the bus of a network or a KOMPYU evening system. For this reason, it is difficult to make regularity delay of the outgoing end of the encoder system 7, and the input edge of the decoder system 9. Hereafter, this problem is explained with reference to drawing 7.

0009 Drawing 7 illustrates the relation between the expected value of the data time of arrival in case an MPEG stream is inputted into a decoder, and the time of arrival on a actual MPEG system. Here, it is premised on transmitting the MPEG stream outputted from an encoder in the unit (a thing like the cell as used in the field of ATM: consider it as fixed length) settled at a certain fixed interval. Under this premise, if the delay of a course until an MPEG stream goes into a decoder is always constant, as shown in drawing 7 (a), the time of arrival of a cell will become fixed. However, transmission of a actual MPEG stream is influenced by various factors (for

example, a network being crowded and the bus inside condition and a video server being crowded condition, data read time from a hard disk). For this reason, as shown in drawing 7 (b), the time of arrival of a cell becomes the thing **time / which is expected** shifted. Thus, it is being called the jitter (fluctuation) that the time of arrival of each cell becomes scattering.

0010 Thus, since a jitter arises in transmission of an MPEG stream, supposing it does not adopt a measure at all, restoration of the exact hour entry in a receiver will become difficult. So, in the MPEG system, the means for removing this jitter is formed in the decoder system of the receiver. Hereafter, the composition is explained with reference to drawing 5.

0011 In the decoder system shown in this drawing 5, in order to remove a jitter, the buffer 5 is formed before the system decoder & demultiplexer 4 which takes out a hour entry from an MPEG stream. MPEG stream VMS (VMS:Variable delay MPEG Stream) having contained the jitter is once accumulated in the buffer 5. And the MPEG stream accumulated in the buffer 5 is read at a fixed rate, serves as MPEG stream CMS (CMS:Constant delayMPEGStream) of the fixed transfer rate which does not contain a jitter, and is outputted by the transfer rate control circuit 6. It shall be beforehand set as the transfer rate control circuit 6 the transfer rate of which an MPEG stream has.

0012 The system decoder & demultiplexer 4 divides MPEG stream CMS into the packet of video and an audio, and sends out each packet to the video decoder 2 and the audio decoder 3. The video decoder 2 decrypts the sent video packet, and sends out video signal DV. Similarly, the audio decoder 3 decrypts the sent audio packet, and outputs audio signal DA.

0013 Now, since video signal DV and audio signal DA are decrypted independently, respectively, both regeneration time shifts from the expected thing only by outputting the only decrypted data. For this reason, if MPEG data which human being has spoken is reproduced for example, the phenomenon in which a motion and voice of a mouth do not suit will happen. So, in MPEG, the regeneration time management information (PTS:Presentation Time Stamp) of video and an audio is given into each packet, In each decoder, when the reference clock (STC:System Time Clock) which a decoder system has is in agreement with PTS, it is made to carry out the reproducing output of the data of the packet.

0014 Here, STC by the side of a decoder must be correctly in agreement with the time reference clock by the side of an encoder. However, even if it is using the same oscillator of the same maker by the encoder and decoder side, a certain error will be a certain thing between each clock by which it is generated by both oscillators. If the data of MPEG is reproduced for a long time even if it is a case so that only the slight gap where both clocks synchronize mostly and are not visible may be produced in the beginning, the gap becomes large, and however it may see before long, a motion and sound of a screen stop therefore, suiting.

0015 In order to amend this gap, in an MPEG stream, it is the time information (in MPEG1 and an MPEG 2 program stream) by the side of an encoder. **SCR:System Clock Reference and** At an MPEG2 transport stream, PCR:Program Clock Reference is minced periodically (see drawing 8 and drawing 9), and the value of SCR or PCR, i.e., the value whose intention the encoder side has, is set to STC by the decoder side. At this time, the accuracy of the arrival time of the MPEG stream included in the decoder side is required.

0016 The example of composition of the clock recovery circuit 1 shown in drawing 6, STC and PLL (Phase Locked.) Loop; the phase comparator 13, the low pass filter 14, and voltage controlled oscillator (VCXO:Voltage-Controlled Crystal Oscillator) 1 It comprises a return closed circuit which comprises 1 etc. It can have with the decoder STC which corresponded with the system clock by the side of an encoder thoroughly by this circuit while amending the gap of STC delicately.

0017 The details of the MPEG system explained above are explained to ISO/IEC DIS 11172-1 and ISO/IEC DIS 13818-1, for example.

0018

Problem to be solved by the invention By the way, the conventional MPEG system mentioned above had the following problem. That is, although the capacity of the buffer 5 formed in the decoder system 9 considers the jitter of MPEG stream VMS expected beforehand and is determined, if this jitter becomes large suddenly for some Reasons, it may be unable to absorb a jitter by the capacity of the buffer 5. And if this situation arises, disorder of a picture or a sound will arise in the video of MPEG, or playback of an audio. It is because this has the very slight width of the clock frequency which can be adjusted by VCXO11 of the clock recovery circuit 1.

0019 Also in the bottom of the situation where this invention is made in view of the situation explained above, and the jitter of the MPEG stream received becomes large suddenly, It is made to synchronize with the clock of the transmitting side, without making the reference clock of the decoder system of a receiver produce a big gap, and aims at providing the MPEG data transfer control circuit which makes it possible to receive the stable MPEG stream.

0020

Means for solving problemA buffer which stores MPEG data in which this invention is received, and a transfer rate control circuit which transmits MPEG data stored in said buffer to a decoder with a fixed transfer rate, Time which time information included in MPEG data read from said buffer and a reference clock used for timing control of said decoder show is compared, Let an MPEG data transfer control circuit possessing a time information comparison circuit which supplies instructions of a purport that said transfer rate should be changed based on a comparison result to said transfer rate control circuit be a summary.

0021

Mode for carrying out the invention Hereafter, an embodiment of the invention is described with reference to Drawings.

0022A. The 1st embodiment drawing 1 is a block diagram showing composition of an MPEG decoder system which applied an MPEG data transfer control circuit which is one embodiment of this invention. This MPEG decoder system is a system carried in a personal computer etc., and plays MPEG contents memorized by hard disk etc.
0023 In drawing 1, the buffer 5 is a means to accumulate MPEG stream VMS sent via a transmission line from an encoder. Here, MPEG stream VMS sent via a transmission line generally contains the JITSU evening. The data stored in the buffer 5 is read with a predetermined transfer rate under control by the transfer rate control circuit 6, serves as MPEG stream CMS, and is supplied to the system decoder & demultiplexer 4.
0024 This system decoder & demultiplexer 4 analyzes MPEG stream CMS, and the video packet in MPEG stream CMS is transmitted to the video decoder 2, and it transmits an audio packet to the audio decoder 3. The system decoder & demultiplexer 4 extracts MPEG stream CMS to SCR or PCR, and gives it to the clock recovery circuit 1 and the time information comparison circuit 21.
0025 The clock recovery circuit 1 is correctly doubled from SCR or PCR extracted by the system decoder & demultiplexer 4 at the time when the encoder meant STC used as the reference clock of an MPEG decoder system. STC currently controlled here is connected with the video decoder 2 and the audio decoder 3 in the time information comparison circuit 21.
0026 The video decoder 2 decodes the video packet taken out by the system decoder & demultiplexer 4, and outputs video signal DV. Decoding of the video packet by this video decoder 2 and the output of video signal DV are performed in the state where it synchronized with the audio signal, according to STC in the clock recovery circuit 1. On the other hand, the audio decoder 3 decodes the audio packet taken out by the system decoder & demultiplexer 4, and outputs audio signal DA. Decoding of the audio packet by this audio decoder 3 and the output of audio signal DA are performed in the state where it synchronized with the video signal, according to STC in the clock recovery circuit 1.
0027 The time information comparison circuit 21 compares SCR, or PCR and STC, and gives the result to the transfer rate control circuit 6. Although it is connected to the buffer 5 and the transfer rate control circuit 6 transmits MPEG stream CMS to the system decoder & demultiplexer 4 from the buffer 5 with the transfer rate set up beforehand, it can change the transfer rate using the information from the transfer rate control circuit 6.
0028 Next, operation of this embodiment is explained. In drawing 1, it uses having stopped catching up with the transfer rate of MPEG stream CMS which MPEG stream VMS inputted into the buffer 5 is overdue, becomes feeling, and is outputted from the buffer 5. In this case, the MPEG stream accumulated into the buffer 5 will decrease gradually, and the buffer 5 will be in sky condition. STC is proofread by the value which the encoder side meant by SCR till then or PCR at this time. However, MPEG stream VMS is inputted into the buffer 5 for the buffer 5 from sky condition after that, MPEG stream CMS is transmitted from the buffer 5, and when the packet having contained SCR or PCR is inputted into the system decoder & demultiplexer 4, this SCR or PCR has with STC a value left greatly.
0029 So, in this embodiment, the transfer rate of MPEG stream CMS outputted from the buffer 5 which compares SCR, or PCR and STC at this time in the time information comparison circuit 21, and is controlled by size of that difference in the transfer rate control circuit is changed. The difference beyond the range which can carry out recovery in the clock recovery circuit 1 by this of SCR, or PCR and STC is promptly recoverable.
0030 Drawing 2 is a time chart showing the relation of the transmission situation and time information of an MPEG stream to this embodiment. Hereafter, concrete operation of this embodiment is explained with reference to drawing 2. In drawing 2, as for the buffer Empty, the buffer 5 shows sky condition. VMS shows the period when MPEG stream VMS is transmitted to the buffer 5. CMS shows the period when MPEG stream CMS is transmitted to the system decoder & demultiplexer 4 from the buffer 5, and it is shown that the portion of a thick line is transmitted to a high speed from the usual transmission. SCR/PCR from which STC was taken out by STC in an MPEG decoder system, and SCR/PCR was taken out by the system decoder & demultiplexer 4 is shown. The easy integer for convenience has described such time information, and it differs from the time information actually treated.
0031 Usually, if nothing happens, MPEG stream VMS is read, being managed so that the buffer 5 may not become empty. If MPEG stream VMS is read into the buffer 5 and the buffer 5 fills, transmission of MPEG stream VMS will no longer be performed. MPEG stream CMS reads the data currently stored in the buffer 5, and continues transmission. If the buffer 5 approaches sky condition, transmission of MPEG stream VMS will be started again. Such operation is repeated and data transfer of MPEG stream CMS is carried out continuously.
0032 The case where MPEG stream VMS would not be transmitted by some causes, and all the data of the buffer 5 has been swept out is considered. If the data of the buffer 5 is lost, MPEG stream CMS will not be transmitted. Also then, STC continues mincing time with a constant interval. Since the day evening will be stored in the buffer 5 if transmission of MPEG stream VMS is resumed, transmission of MPEG stream CMS starts again. Although the system decoder & demultiplexer 4 detects SCR or PCR, since SCR or PCR detected here must be in agreement with STC immediately after transmission of MPEG stream CMS breaks off from the first, STC in this time serves as a value left greatly. In the example, it is SCR/PCR=6 in the hit which passed over STC=7.
0033 Now, in an already explained Prior art, STC is delicately adjusted by the clock recovery circuit 1 (when it is this embodiment, adjusted in the direction which makes a clock late.), and STC, and SCR or PCR becomes the same value gradually.
0034 On the other hand, in this embodiment, it is detected that STC, and SCR or PCR is greatly shifted by the time information comparison circuit 21, When what STC is following from SCR or PCR (it is got blocked and a value is large) is understood, the time information comparison circuit 21 notifies it to the transfer rate control

circuit 6. This is performed until a value of SCR or PCR catches up with a value of STC mostly. This time is dramatically short compared with a conventional method.

0035 About video of this period, and playback of an audio, data which remains in the system decoder & demultiplexer 4 and the video decoder 2, and the audio decoder 3 before this is played. Namely, in a circuit which actually constitutes these system decoder & demultiplexers. A packet prepared in order to connect a memory and to transmit to a memory of the system decoder & demultiplexer 4 at each decoder for the number packet of MPEG stream CMS, Data (it is the image data for several frames in the case of the video decoder 2) prepared in order to output to a memory of each decoder with a packet before decrypting remains. Therefore, what is necessary is just to reproduce these remaining data in the above-mentioned period.

0036 As mentioned above, although a case where a value of SCR and PCR was overdue to a value of STC was explained, when a value of SCR or PCR progresses to a value of STC conversely, operation that the transfer rate control circuit 6 delays a transfer rate of MPEG stream CMS is performed.

0037 According to this embodiment described above, the following effects are acquired.

(1) Since MPEG stream CMS is transmitted to a high speed until the difference is lost mostly when SCR or PCR is greatly late compared with STC, a value of SCR or PCR can be made to catch up with STC early.

(2) As mentioned above, in order that a value of SCR or PCR may catch up with STC quickly, a period when a cycle of STC is confused is short. Therefore, a picture or a sound under reproduction is overdue, and it does not become feeling.

0038B. The 2nd embodiment drawing 3 is a block diagram showing composition of a 2nd embodiment of this invention. This embodiment connects the time information store circuit 22 to the time information comparison circuit 21 in a 1st embodiment (drawing 1) of the above, Are and it receives it made to deliver a comparison result (difference information) of STC, and SCR or PCR which the system decoder & demultiplexer 4 extracted between the time information comparison circuit 21 and this time information store circuit 22. It is as follows when it furthermore explains in full detail.

0039 First, the time information comparison circuit 21 is always comparing SCR, or PCR and STC, and it writes periodically the difference information of the comparison result, i.e., the time which SCR or PCR shows, and the time which STC shows in the time information store circuit 22 (for example, when STC changes). The time information comparison circuit 21 reads before the difference information of the time written in the time information store circuit 22, when comparing SCR, or PCR and STC.

0040 It is judged whether the difference information of the present time and the difference information of former time open the time information comparison circuit 21, it looks at condition, and is following whether the value of present SCR or PCR is behind for some time compared with STC. Since how many times of past a minute of comparison result is compared, and it understands what% it should advance the transfer rate of the MPEG stream CMS which opens and is flowing from condition now when it seems that it is behind, Only the rate sets up the transfer rate of MPEG stream CMS early to the transfer rate control circuit 6. Since transmission of MPEG stream CMS is performed with the transfer rate newly set as the transfer rate control circuit 6, it has stopped opening the difference of SCR, and PCR and STC opened little by little until now rather than before. Supposing similarly SCR or PCR is opening in the direction which progresses rather than STC, the time information comparison circuit 21 will set up a transfer rate delay the transfer rate of MPEG stream CMS to the transfer rate control circuit 6. When the difference information of the past SCR or the time of PCR and STC progresses or it is behind, the time information comparison circuit 21 does not newly set up a transfer rate to the transfer rate control circuit 6.

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Effect of the Invention As explained above, according to the MPEG data transfer control circuit concerning this invention. It is made to synchronize with the clock of the transmitting side, without making the reference clock of the decoder system of a receiver produce a big gap under the situation where the jitter of the MPEG stream received becomes large suddenly, and is effective in the stable MPEG stream being receivable.

Field of the Invention This invention relates to the MPEG data transfer control circuit for performing control for supplying to a decoder the MPEG data which is applied to an MPEG decoder, especially is received via a transmission line at a fixed rate.

Description of the Prior Art As the International Standard about digital video (video) coding (compression), voice (audio) coding, and its multiplex and separation system, There is an MPEG (Moving PictureExperts Group) standard (ISO/IEC DIS 11172/13818) used in common in fields, such as a storage medium, communication, and broadcast. MPEG1 used for this MPEG standard by storage media, such as CD-ROM (CompactDisk Read Only Memory), There is MPEG 2 which broadcast and the use in a telecommunications sector besides the application of this MPEG1 are considered, and is used with broad application. The MPEG 2 program stream (PS:ProgramStream) which can constitute one program in a stream like **this MPEG 2** MPEG1, There are two kinds of systems called the MPEG2 transport stream (TS:Transport Stream) which can constitute two or more programs in a stream. Since especially MPEG 2-TS can summarize two or more programs to one stream, it can respond to television broadcasting etc. MPEG 2-TS is provided with flexibility, a scramble function, etc. of

program organization so that it may harness this advantage.

0003 Next, the MPEG system which performs the data communications corresponding to MPEG explained above is explained. In this MPEG system, the video signal and audio signal which digitized at the transmitting side are compressed once, and it transmits to a receiver through media, such as a network and a hard disk. And in a receiver, the original video signal and audio signal are restored from the compressed data. Here, irreversible encoding is used for the coding mode of MPEG in order to drop the amount of information as much as possible. For this reason, in a receiver, the original video signal and audio signal cannot be restored thoroughly. However, using well the weak point of human being's vision and an acoustic sense, the amount of information is dropped on the coding mode of MPEG to such an extent that he hardly notices human being. However, if the transfer rate of the MPEG day evening becomes low (it is got blocked and the amount of information becomes small), the difference with the original image and fundamental tone voice which can be checked to human being will become large. The above is an outline of an MPEG system.

0004 Drawing 4 is a block diagram showing the basic constitution of the MPEG system explained above. Drawing 5 is a block diagram showing the example of composition of the decoder system 9 in an MPEG system. Drawing 6 is a block diagram showing the composition of the clock recovery 1 in the decoder system 9.

0005 In drawing 4, the MPEG encoder system 7 includes an encoder, a buffer, a clock control circuit, etc. Audio input A.I. Artificial Intelligence which is input video VI and the audio signal which are picture signals is inputted into this encoder system 7. And the MPEG encoder system 7 compresses these input, and outputs the compressed MPEG stream (MPEG coding was carried out). This MPEG stream is inputted into the MPEG decoder system 9 through a network or the video server 8. The MPEG decoder system 9 decodes these compression streams, and outputs the video output VO and the audio output AO.

0006 By the way, in an MPEG system, signal transmission between the input edge of the MPEG encoder system 7 and the outgoing end of the MPEG decoder system 9 must always be performed by fixed delay. Because, it is necessary to transmit a video signal and an audio signal to real time by a waveform as it is in an MPEG system. For example, when its attention is paid to the video or the audio signal inputted into the encoder system 7, Each signal exactly inputted into ... in 1 second, 2 seconds, and 3 seconds from the input start point in time of a top signal must be exactly outputted to ... in 1 second, 2 seconds, and 3 seconds from the output start point in time of a top signal, also when outputted from the decoder system 9.

0007 In an MPEG system, signal transmission between the outgoing end of the encoder system 7 and the input edge of the decoder system 9 must also always be performed by fixed delay. Because, include the time information (time information intended with the encoder) as which the encoder system 7 expresses the timing of the clock by the side of an encoder in an MPEG system into an MPEG stream, and it transmits, In the decoder system 9, the reference clock used for control of the reproducing output timing of video or an audio is synchronized with the clock by the side of an encoder by receiving this time information (in addition, this synchronization control is mentioned later). Therefore, if the delay of the signal transmission between the outgoing end of the encoder system 7 and the input edge of the decoder system 9 is not fixed, the receiving timing of the hour entry in the decoder system 9 will come apart, and the reference clock by the side of a decoder will shift from the clock by the side of an encoder. Unless signal transmission between the outgoing end of the encoder system 7 and the input edge of the decoder system 9 is performed for fixed delay, signal transmission between the input edge of the MPEG encoder system 7 and the outgoing end of the MPEG decoder system 9 cannot be performed for fixed delay, either. Therefore, signal transmission between the outgoing end of the encoder system 7 and the input edge of the decoder system 9 must always be performed for fixed delay as above-mentioned.

0008 However, transmission of an MPEG stream is actually performed through the bus of a network or a KOMPYU evening system. For this reason, it is difficult to make regularity delay of the outgoing end of the encoder system 7, and the input edge of the decoder system 9. Hereafter, this problem is explained with reference to drawing 7.

0009 Drawing 7 illustrates the relation between the expected value of the data time of arrival in case an MPEG stream is inputted into a decoder, and the time of arrival on a actual MPEG system. Here, it is premised on transmitting the MPEG stream outputted from an encoder in the unit (a thing like the cell as used in the field of ATM: consider it as fixed length) settled at a certain fixed interval. Under this premise, if the delay of a course until an MPEG stream goes into a decoder is always constant, as shown in drawing 7 (a), the time of arrival of a cell will become fixed. However, transmission of a actual MPEG stream is influenced by various factors (for example, a network being crowded and the bus inside condition and a video server being crowded condition, data read time from a hard disk). For this reason, as shown in drawing 7 (b), the time of arrival of a cell becomes the thing **time / which is expected** shifted. Thus, it is being called the jitter (fluctuation) that the time of arrival of each cell becomes scattering.

0010 Thus, since a jitter arises in transmission of an MPEG stream, supposing it does not adopt a measure at all, restoration of the exact hour entry in a receiver will become difficult. So, in the MPEG system, the means for removing this jitter is formed in the decoder system of the receiver. Hereafter, the composition is explained with reference to drawing 5.

0011 In the decoder system shown in this drawing 5, in order to remove a jitter, the buffer 5 is formed before the system decoder & demultiplexer 4 which takes out a hour entry from an MPEG stream. MPEG stream VMS (VMS:Variable delay MPEG Stream) having contained the jitter is once accumulated in the buffer 5. And the MPEG stream accumulated in the buffer 5 is read at a fixed rate, serves as MPEG stream CMS (CMS:Constant delayMPEGStream) of the fixed transfer rate which does not contain a jitter, and is outputted by the transfer rate control circuit 6. It shall be beforehand set as the transfer rate control circuit 6 the transfer rate of which an

MPEG stream has.
0012 The system decoder & demultiplexer 4 divides MPEG stream CMS into the packet of video and an audio, and sends out each packet to the video decoder 2 and the audio decoder 3. The video decoder 2 decrypts the sent video packet, and sends out video signal DV. Similarly, the audio decoder 3 decrypts the sent audio packet, and outputs audio signal DA.
0013 Now, since video signal DV and audio signal DA are decrypted independently, respectively, both regeneration time shifts from the expected thing only by outputting the only decrypted data. For this reason, if MPEG data which human being has spoken is reproduced for example, the phenomenon in which a motion and voice of a mouth do not suit will happen. So, in MPEG, the regeneration time management information (PTS:Presentation Time Stamp) of video and an audio is given into each packet, In each decoder, when the reference clock (STC:System Time Clock) which a decoder system has is in agreement with PTS, it is made to carry out the reproducing output of the data of the packet.
0014 Here, STC by the side of a decoder must be correctly in agreement with the time reference clock by the side of an encoder. However, even if it is using the same oscillator of the same maker by the encoder and decoder side, a certain error will be a certain thing between each clock by which it is generated by both oscillators. If the data of MPEG is reproduced for a long time even if it is a case so that only the slight gap where both clocks synchronize mostly and are not visible may be produced in the beginning, the gap becomes large, and however it may see before long, a motion and sound of a screen stop therefore, suiting.
0015 In order to amend this gap, in an MPEG stream, it is the time information (in MPEG1 and an MPEG 2 program stream) by the side of an encoder. **SCR:System Clock Reference and** At an MPEG2 transport stream, PCR:Program Clock Reference is minced periodically (see drawing 8 and drawing 9), and the value of SCR or PCR, i.e., the value whose intention the encoder side has, is set to STC by the decoder side. At this time, the accuracy of the arrival time of the MPEG stream included in the decoder side is required.
0016 The example of composition of the clock recovery circuit 1 shown in drawing 6, STC and PLL (Phase Locked.) Loop; the phase comparator 13, the low pass filter 14, and voltage controlled oscillator (VCXO:Voltage-Controlled Crystal Oscillator) 1 It comprises a return closed circuit which comprises 1 etc. It can have with the decoder STC which corresponded with the system clock by the side of an encoder thoroughly by this circuit while amending the gap of STC delicately.
0017 The details of the MPEG system explained above are explained to ISO/IEC DIS 11172-1 and ISO/IEC DIS 13818-1, for example.

Effect of the Invention As explained above, according to the MPEG data transfer control circuit concerning this invention. It is made to synchronize with the clock of the transmitting side, without making the reference clock of the decoder system of a receiver produce a big gap under the situation where the jitter of the MPEG stream received becomes large suddenly, and is effective in the stable MPEG stream being receivable.

Problem to be solved by the invention By the way, the conventional MPEG system mentioned above had the following problem. That is, although the capacity of the buffer 5 formed in the decoder system 9 considers the jitter of MPEG stream VMS expected beforehand and is determined, if this jitter becomes large suddenly for some Reasons, it may be unable to absorb a jitter by the capacity of the buffer 5. And if this situation arises, disorder of a picture or a sound will arise in the video of MPEG, or playback of an audio. It is because this has the very slight width of the clock frequency which can be adjusted by VCXO11 of the clock recovery circuit 1.
0019 Also in the bottom of the situation where this invention is made in view of the situation explained above, and the jitter of the MPEG stream received becomes large suddenly, It is made to synchronize with the clock of the transmitting side, without making the reference clock of the decoder system of a receiver produce a big gap, and aims at providing the MPEG data transfer control circuit which makes it possible to receive the stable MPEG stream.

Means for solving problem The buffer which stores the MPEG data in which this invention is received, and the transfer rate control circuit which transmits the MPEG data stored in said buffer to a decoder with a fixed transfer rate, The time which the time information included in the MPEG data read from said buffer and the reference clock used for the timing control of said decoder show is compared, Let the MPEG data transfer control circuit possessing the time information comparison circuit which supplies instructions of the purport that said transfer rate should be changed based on a comparison result to said transfer rate control circuit be a summary.
0021
Mode for carrying out the invention Hereafter, an embodiment of the invention is described with reference to Drawings.
0022A. The 1st embodiment drawing 1 is a block diagram showing the composition of the MPEG decoder system which applied the MPEG data transfer control circuit which is one embodiment of this invention. This MPEG decoder system is a system carried in a personal computer etc., and plays the MPEG contents memorized by the

hard disk etc.

0023 In drawing 1, the buffer 5 is a means to accumulate MPEG stream VMS sent via a transmission line from an encoder. Here, MPEG stream VMS sent via a transmission line generally contains the JITSU evening. The data stored in the buffer 5 is read with a predetermined transfer rate under control by the transfer rate control circuit 6, serves as MPEG stream CMS, and is supplied to the system decoder & demultiplexer 4.

0024 This system decoder & demultiplexer 4 analyzes MPEG stream CMS, and the video packet in MPEG stream CMS is transmitted to the video decoder 2, and it transmits an audio packet to the audio decoder 3. The system decoder & demultiplexer 4 extracts MPEG stream CMS to SCR or PCR, and gives it to the clock recovery circuit 1 and the time information comparison circuit 21.

0025 The clock recovery circuit 1 is correctly doubled from SCR or PCR extracted by the system decoder & demultiplexer 4 at the time when the encoder meant STC used as the reference clock of an MPEG decoder system. STC currently controlled here is connected with the video decoder 2 and the audio decoder 3 in the time information comparison circuit 21.

0026 The video decoder 2 decodes the video packet taken out by the system decoder & demultiplexer 4, and outputs video signal DV. Decoding of the video packet by this video decoder 2 and the output of video signal DV are performed in the state where it synchronized with the audio signal, according to STC in the clock recovery circuit 1. On the other hand, the audio decoder 3 decodes the audio packet taken out by the system decoder & demultiplexer 4, and outputs audio signal DA. Decoding of the audio packet by this audio decoder 3 and the output of audio signal DA are performed in the state where it synchronized with the video signal, according to STC in the clock recovery circuit 1.

0027 The time information comparison circuit 21 compares SCR, or PCR and STC, and gives the result to the transfer rate control circuit 6. Although it is connected to the buffer 5 and the transfer rate control circuit 6 transmits MPEG stream CMS to the system decoder & demultiplexer 4 from the buffer 5 with the transfer rate set up beforehand, it can change the transfer rate using the information from the transfer rate control circuit 6.

0028 Next, operation of this embodiment is explained. In drawing 1, it uses having stopped catching up with the transfer rate of MPEG stream CMS which MPEG stream VMS inputted into the buffer 5 is overdue, becomes feeling, and is outputted from the buffer 5. In this case, the MPEG stream accumulated into the buffer 5 will decrease gradually, and the buffer 5 will be in sky condition. STC is proofread by the value which the encoder side meant by SCR till then or PCR at this time. However, MPEG stream VMS is inputted into the buffer 5 for the buffer 5 from sky condition after that, MPEG stream CMS is transmitted from the buffer 5, and when the packet having contained SCR or PCR is inputted into the system decoder & demultiplexer 4, this SCR or PCR has with STC a value left greatly.

0029 So, in this embodiment, the transfer rate of MPEG stream CMS outputted from the buffer 5 which compares SCR, or PCR and STC at this time in the time information comparison circuit 21, and is controlled by size of that difference in the transfer rate control circuit is changed. The difference beyond the range which can carry out recovery in the clock recovery circuit 1 by this of SCR, or PCR and STC is promptly recoverable.

0030 Drawing 2 is a time chart showing the relation of the transmission situation and time information of an MPEG stream to this embodiment. Hereafter, concrete operation of this embodiment is explained with reference to drawing 2. In drawing 2, as for the buffer Empty, the buffer 5 shows sky condition. VMS shows the period when MPEG stream VMS is transmitted to the buffer 5. CMS shows the period when MPEG stream CMS is transmitted to the system decoder & demultiplexer 4 from the buffer 5, and it is shown that the portion of a thick line is transmitted to a high speed from the usual transmission. SCR/PCR from which STC was taken out by STC in an MPEG decoder system, and SCR/PCR was taken out by the system decoder & demultiplexer 4 is shown. The easy integer for convenience has described such time information, and it differs from the time information actually treated.

0031 Usually, if nothing happens, MPEG stream VMS is read, being managed so that the buffer 5 may not become empty. If MPEG stream VMS is read into the buffer 5 and the buffer 5 fills, transmission of MPEG stream VMS will no longer be performed. MPEG stream CMS reads the data currently stored in the buffer 5, and continues transmission. If the buffer 5 approaches sky condition, transmission of MPEG stream VMS will be started again. Such operation is repeated and data transfer of MPEG stream CMS is carried out continuously.

0032 The case where MPEG stream VMS would not be transmitted by some causes, and all the data of the buffer 5 has been swept out is considered. If the data of the buffer 5 is lost, MPEG stream CMS will not be transmitted. Also then, STC continues mincing time with a constant interval. Since the day evening will be stored in the buffer 5 if transmission of MPEG stream VMS is resumed, transmission of MPEG stream CMS starts again. Although the system decoder & demultiplexer 4 detects SCR or PCR, since SCR or PCR detected here must be in agreement with STC immediately after transmission of MPEG stream CMS breaks off from the first, STC in this time serves as a value left greatly. In the example, it is SCR/PCR=6 in the hit which passed over STC=7.

0033 Now, in the already explained Prior art, STC is delicately adjusted by the clock recovery circuit 1 (when it is this embodiment, adjusted in the direction which makes a clock late.), and STC, and SCR or PCR becomes the same value gradually.

0034 On the other hand, in this embodiment, it is detected that STC, and SCR or PCR is greatly shifted by the time information comparison circuit 21, When what STC is following from SCR or PCR (it is got blocked and a value is large) is understood, the time information comparison circuit 21 notifies it to the transfer rate control circuit 6. This is performed until the value of SCR or PCR catches up with the value of STC mostly. This time is dramatically short compared with the conventional method.

0035 About the video of this period, and playback of an audio, the data which remains in the system decoder &

demultiplexer 4 and the video decoder 2, and the audio decoder 3 before this is played. Namely, in the circuit which actually constitutes these system decoder & demultiplexers. The packet prepared in order to connect the memory and to transmit to the memory of the system decoder & demultiplexer 4 at each decoder for the number packet of MPEG stream CMS, The data (it is the image data for several frames in the case of the video decoder 2) prepared in order to output to the memory of each decoder with the packet before decrypting remains. Therefore, what is necessary is just to reproduce these remaining data in the above-mentioned period.

0036 As mentioned above, although the case where the value of SCR and PCR was overdue to the value of STC was explained, when the value of SCR or PCR progresses to the value of STC conversely, operation that the transfer rate control circuit 6 delays the transfer rate of MPEG stream CMS is performed.

0037 According to this embodiment described above, the following effects are acquired.

(1) Since MPEG stream CMS is transmitted to a high speed until the difference is lost mostly when SCR or PCR is greatly late compared with STC, the value of SCR or PCR can be made to catch up with STC early.

(2) As mentioned above, in order that the value of SCR or PCR may catch up with STC quickly, the period when the cycle of STC is confused is short. Therefore, the picture or sound under reproduction is overdue, and it does not become feeling.

0038B. The 2nd embodiment drawing 3 is a block diagram showing the composition of a 2nd embodiment of this invention. This embodiment connects the time information store circuit 22 to the time information comparison circuit 21 in a 1st embodiment (drawing 1) of the above, Are and it receives it made to deliver the comparison result (difference information) of STC, and SCR or PCR which the system decoder & demultiplexer 4 extracted between the time information comparison circuit 21 and this time information store circuit 22. It is as follows when it furthermore explains in full detail.

0039 First, the time information comparison circuit 21 is always comparing SCR, or PCR and STC, and it writes periodically difference information of the comparison result, i.e., time which SCR or PCR shows, and time which STC shows in the time information store circuit 22 (for example, when STC changes). The time information comparison circuit 21 reads before difference information of time written in the time information store circuit 22, when comparing SCR, or PCR and STC.

0040 It is judged whether difference information of the present time and difference information of former time open the time information comparison circuit 21, it looks at condition, and is following whether a value of present SCR or PCR is behind for some time compared with STC. Since how many times of past a minute of comparison result is compared, and it understands what% it should advance a transfer rate of the MPEG stream CMS which opens and is flowing from condition now when it seems that it is behind, Only the rate sets up a transfer rate of MPEG stream CMS early to the transfer rate control circuit 6. Since transmission of MPEG stream CMS is performed with a transfer rate newly set as the transfer rate control circuit 6, it has stopped opening a difference of SCR, and PCR and STC opened little by little until now rather than before. Supposing similarly SCR or PCR is opening in the direction which progresses rather than STC, the time information comparison circuit 21 will set up a transfer rate delay a transfer rate of MPEG stream CMS to the transfer rate control circuit 6. When difference information of the past SCR or time of PCR and STC progresses or it is behind, the time information comparison circuit 21 does not newly set up a transfer rate to the transfer rate control circuit 6.

Brief Description of the Drawings

Drawing 1 It is a block diagram showing the composition of the MPEG decoder system which applied the MPEG data transfer control circuit which is a 1st embodiment of this invention.

Drawing 2 It is a time chart which shows operation of the embodiment in contrast with conventional technology.

Drawing 3 It is a block diagram showing the composition of the MPEG decoder system which applied the MPEG data transfer control circuit which is a 2nd embodiment of this invention.

Drawing 4 It is a block diagram showing the composition of a common MPEG system.

Drawing 5 It is a block diagram showing the composition of the conventional MPEG decoder system.

Drawing 6 It is a block diagram showing the example of composition of the clock recovery circuit in the conventional MPEG decoder system.

Drawing 7 It is a figure which illustrates the transmission forms of the cell in an MPEG system.